DESIGNCON® 2026
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A Hybrid System-Level Modeling and Sensitivity Analysis Approach to Improve IC Immunity for Inductive Positioning Sensors in Noisy Automotive Environments

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Information Classification: General

Abstract

Integrated circuit (IC) immunity failures in automotive and industrial systems are often the result of unintended noise coupling from complex harnesses and passive components that propagate disturbances directly to IC pins. Despite growing concerns in EMC design, the noise susceptibility of ICs is rarely considered during the early phases of IC or system design. This gap largely stems from the absence of accurate system-level estimation and impact analysis methods that capture how injected noise translates into IC-level disturbances. The challenge arises due to the complex nature of the system, which includes wire harnesses, non-linear components—such as current-injecting clamps—printed circuit boards (PCBs), active and passive circuits, and noise injection paths. In the following work, we demonstrate that these challenges can be addressed using a hybrid modeling approach, combining full-wave electromagnetic simulations based on the Method of Moments (MoM) with network-based system modeling techniques. Key elements, such as injection clamps, termination networks, and passive components, are modeled with equivalent circuit representations, while active circuits are characterized using their impedance profiles and IC Immunity Models (ICIM) derived from Direct Power Injection (DPI) measurements.

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Introduction

Integrated circuit (IC) immunity failures in automotive and industrial electronic systems often originate from unintended electromagnetic (EM) noise coupling, primarily through complex wire harnesses, printed circuit boards (PCBs), and passive components [1], [2]. These pathways can propagate high-frequency disturbances directly to sensitive IC pins, leading to functional disruptions such as incorrect signal interpretation, output errors, or complete malfunctions. Although electromagnetic compatibility (EMC) is a growing concern—particularly in the early stages of system and IC development—IC noise susceptibility is frequently overlooked during design and verification phases due to the lack of predictive system-level modelling techniques [2], [3].

One of the core challenges lies in the multi-domain nature of modern electronic systems, which include nonlinear elements such as current-injecting clamps, mode-converting PCBs, inductive sensors, and termination networks [3], [4], [9]. These systems are exposed to broadband conducted and radiated disturbances, especially in environments with high-speed digital and power electronics. Modelling such interactions is difficult due to the interplay of EM fields, circuit parasitics, and nonlinear device behaviour [3], [8].

To bridge this gap, recent work has explored hybrid modelling approaches that combine full-wave electromagnetic (EM) solvers—such as the Method of Moments (MoM) or Finite Element Method (FEM)—with circuit-level network simulations [4], [8], [9]. In this methodology, large passive structures like injection probes and harnesses are modelled using full-wave EM techniques, while active and nonlinear circuits are represented via behavioural models or measured impedance profiles [5], [6]. A particularly useful technique in this context is the IC Immunity Model (ICIM), derived from Direct Power Injection (DPI) measurements, which enables passive modelling of otherwise nonlinear IC behaviour in the frequency domain [6], [7].

The DPI method allows us to empirically determine the voltage or power thresholds at which an IC begins to exhibit functional failure [11]. These thresholds are then used as frequency-dependent pass/fail criteria in system-level simulations, enabling the translation of transient-level IC behaviour into AC-domain EMC simulations, such as those performed during Bulk Current Injection (BCI) testing [1], [2].

A particularly vulnerable subsystem in this context is the inductive sensor, widely used in automotive and industrial applications for position or proximity detection [2], [7]. Inductive sensors operate by generating a controlled EM field, which is perturbed by nearby metallic objects. The sensor's output is derived from this perturbation and is highly sensitive to any interference in the field. While these sensors incorporate shielding and integrated electronics to suppress external noise, they remain susceptible to high-frequency common-mode (CM) disturbances, especially during BCI tests [2], [3], [7].

In a typical failure scenario, a common-mode noise current is injected through a wire harness and reaches the PCB, where asymmetries in layout parasitics or sensor geometry convert part of this CM energy into differential-mode (DM) voltage [3], [4], [9]. This DM voltage may then appear across the sensor's signal lines, or the IC input pins, potentially triggering a failure if it exceeds the IC's immunity threshold. Furthermore, at higher frequencies, parasitic capacitive coupling between the sensor's shield and nearby structures (e.g., the test table or ground plane) creates a low impedance return path that exacerbates this mode conversion effect [7].

Because such failures are strongly dependent on layout parasitics, resonance conditions, and small component tolerances, simulation-based diagnosis and optimization become essential tools [3], [4], [7], [9], [10]. Frequency-domain simulations allow engineers to systematically evaluate the induced voltage levels, identify resonant peaks, and apply sensitivity analysis to isolate the most impactful passive components in the design. Combined with DPI-derived immunity thresholds, this enables a predictive framework for BCI pass/fail behaviour, even before physical testing [2], [6], [7], [11].

Simulation Approach

Traditionally, IC simulation is carried out in a SPICE-level environment in which transient phenomena across transistor junctions (including nonlinear effects, switching, charge storage, etc.) are explicitly modelled. In contrast, EMC analyses are conducted in the AC/small-signal (frequency-domain) domain, where nonlinear devices like ICs are often abstracted into their passive impedance representations (i.e. linearized input/output admittances or S-parameters).

In EMC, a major challenge is to map transient functional failures (e.g. bit errors, incorrect detection, wrong output voltage) under electromagnetic excitation into the frequency domain. This problem is particularly important in BCI (Bulk Current Injection) testing, where functional failure is not simply over-voltage, but misbehaviour under EM influence. In other words, BCI failure is inherently a functional behaviour under EM stress, not just a breakdown event. Therefore, the transient nonlinear behaviour must be decoupled from the AC domain and embedded in an AC (frequency domain) simulation. This is commonly achieved via a DPI (Direct Power Injection) measurement that captures the failure threshold (voltage or power) at IC pins and scales it into a lookup table for BCI simulation. During the BCI simulation, the induced differential (or pin) voltage is compared to this threshold table to decide pass or fail.

This section describes this approach and then discusses two optimization paths: (a) inside-IC mitigation (e.g. on-chip capacitors or protection diodes) and (b) board-level mitigation. We focus on board-level design: common-mode to differential conversion (mode conversion), parasitic resonances, and using sensitivity analysis to identify the most sensitive components.

DPI Measurement and Threshold (IB) Extraction

In the DPI method (per IEC 62132-4) shown in Figure 1, RF energy is injected into an IC pin via a coupling network (typically a 50Ω source and a coupling capacitor). The current and voltage at the pin are measured directly to avoid reflection ambiguity.

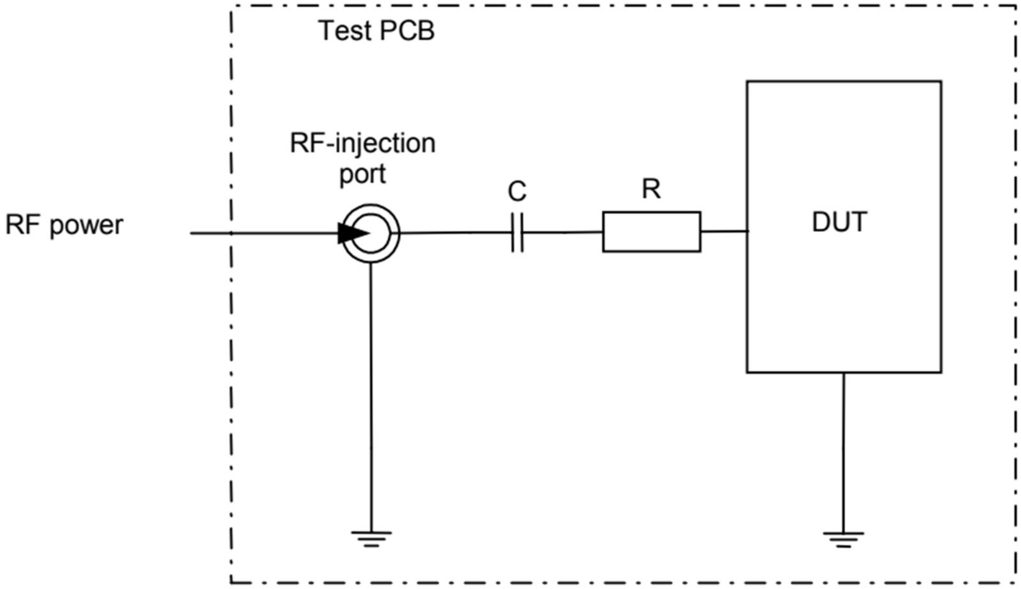


Figure 1. Single IC Pin, Power Injection Principle (IEC 62132-4) [11]

Let $V_{\text{pin}}(f)$ and $I_{\text{pin}}(f)$ be the measured voltage and current at that pin. We define the **impedance** as,

$$Z_{\text{IC}}(f) = \frac{V_{\text{pin}}(f)}{I_{\text{pin}}(f)}$$

We also define the **failure threshold** (IB) at that pin, $V_{\text{fail}}(f)$, which is the maximum RF voltage (or, equivalently, power) at which the IC still operates correctly. That threshold is converted to an equivalent power threshold:

$$P_{\text{fail}}(f) = \frac{|\,V_{\text{fail}}(f)\,|^2}{\{Z_{\text{IC}}(f)\}}$$

Embedding IB into BCI Simulation

In BCI-level simulation, we then treat the IC pin as a **linear impedance** $Z_{\text{IC}}(f)$, and use $V_{\text{fail}}(f)$ as a frequency-dependent “barrier” (lookup table).

In a BCI-style board-level simulation, we inject a **common-mode disturbance** into the cable harness or board ports and compute the **induced differential voltage** at the IC pin, say $V_{\text{ind}}(f)$. Then we compare,

$$|\, V_{\text{ind}}(f) \,| > |\, V_{\text{fail}}(f) \,|$$

If the induced voltage exceeds the threshold at any frequency, a failure is flagged (functional error). Because everything is now linear in the frequency domain (except the threshold condition), we can perform full AC frequency-domain simulations (e.g. S-parameter solvers, circuit + EM co-simulation) to find the failing frequency bands.

Thus, the originally nonlinear phenomenon (IC malfunction) is “reduced” to a frequency-dependent threshold.

Board-Level Mode Conversion via Parasitics

In practice, many EMC failures occur because a **common-mode** noise source (e.g. on a cable) is partially converted into **differential mode** voltage at the IC pin. This **mode conversion** arises due to asymmetries in parasitic layout—slight mismatch in stray capacitance, inductance, trace geometry, ground return path, etc.

Let $Z_{\text{cm}\to\text{diff}}(f)$ denote the impedance transfer function from common-mode excitation to differential voltage at the IC interface. Then,

$$V_{\text{ind}}(f) = Z_{\text{cm}\to\text{diff}}(f)\, I_{\text{cm}}(f)$$

The magnitude and frequency behaviour of $Z_{\text{cm}\to\text{diff}}$ depends heavily on parasitics.

Because parasitic differences are unintended and small, it's extremely difficult to intuitively guess which layout elements (which decoupling caps, ground connections, stray inductances) dominate mode conversion.

Resonant Peaks and Damping

Another aggravating factor is resonance: certain parts of the board (combinations of inductance and capacitance) may resonate at specific frequencies and thus draw large currents, amplifying mode conversion.
In many boards, there are multiple decoupling and filter capacitors. The questions then become:

1. Which component(s) are most responsible for a resonance mode?
2. What is the optimal value (or damping) to shift or suppress that resonance?

A classical lumped model is:

$$Z_{\text{para}}(f) = j\,\omega L_{\text{eq}} + \frac{1}{j\omega C_{\text{eq}}} + R_{\text{damp}}$$

Resonance occurs when $\omega_0 = 1/\sqrt{L_{\text{eq}}C_{\text{eq}}}$. Introducing a damping resistor R_{damp} lowers the quality factor Q, reducing the peak amplitude.

However, in a real board, there are many capacitors (C₁, C₂, …, C_n), inductances, vias, and distributions. Manually creating multiple ports and iteratively changing values is intractable when n is large.

Sensitivity Analysis for EMI/BCI

To systematically identify the most critical components, sensitivity analysis is used. We define the failure metric $F(f)$ as the induced differential pin voltage (or ratio to threshold). Then the sensitivity of F with respect to component k (say capacitor C_k) is,

$$S_k(f) = \frac{\partial F(f)}{\partial C_k}$$

or normalized form,

$$S_k^{\text{norm}}(f) = \frac{C_k}{F(f)} \frac{\partial F(f)}{\partial C_k}$$

At each frequency f, components are ranked by $|\ S_k(f)\ |$. A high sensitivity means a small perturbation in C_k, which significantly influences the induced voltage (hence, failure). Because different components may be sensitive at different frequencies, the sensitivity is frequency-dependent.

In the simplest linear approximation (assuming components are independent), each component's effect can be treated in isolation, i.e.

$$\Delta F \approx \sum_k S_k \, \Delta C_k \, .$$

In practice, we apply small perturbations (e.g. ±10 % in C_k) in the AC simulation and compute the resulting change in $V_{\text{ind}}(f)$. Components with large S_k are prime candidates for redesign or damping.

Example and Discussion

In a real automotive product (for instance a LIN or sensor interface), the method has been demonstrated. DPI is used to derive $V_{\text{fail}}(f)$ for the IC. Then in board-level EMI simulation, we inject a common-mode disturbance (e.g. through the cable) and simulate via full EM/circuit co-simulation the induced differential voltage at the IC pin. Sensitivity analysis is carried out over all decoupling/filter capacitors and a few capacitors with high sensitivity are retuned or damped to shift or suppress resonances. The result is that the previously predicted BCI failure frequency shifts out of the vulnerable band.

One caveat: the assumption of independence between components holds only approximately. Coupling among nearby components may lead to nonlinear interactions in sensitivity. Still, sensitivity ranking provides a powerful heuristic to reduce the search space.

Numerical Results

Inductive Positioning Sensor: Overview

Inductive position sensors are designed to measure the position or displacement of a target object with exceptional accuracy and reliability. These sensors function by generating an alternating magnetic field through a coil. When a conductive target, such as a metal object, enters this magnetic field, eddy currents are induced within the target. These eddy currents produce secondary magnetic fields that interact with the original field, resulting in measurable changes to the coil's impedance.

By analyzing these impedance changes, the sensor can accurately determine the position of the target. Eddy current-based inductive position sensors are commonly utilized in industrial automation, automotive systems, and robotics due to their non-contact operation, robust durability, and ability to perform reliably in challenging environments. They are particularly well-suited for detecting the position of metallic objects and are recognized for their high resolution and rapid response times. These sensors are available in linear, rotary, and arc configurations to accommodate various position sensing requirements. These sensors must comply with stringent immunity requirements in the automotive industry.

Simulation Setup

Bulk Current Injection (BCI) is a complex simulation that requires combined full-wave and circuit-level modeling. The PCB harness is modeled using the Method of Moments (MoM) and all passive components are represented with their parasitic parameters.

Nonlinear components, such as ICs, are modeled using their off-state passive impedance. The BCI injection clamp is represented using a network model. The power calibration and the BCI measurement settings are internally computed. The simulation tool Compliance-Scope [10] is used to execute the BCI analysis and debugging flow. The simulation models used for the BCI system setup are shown in Figure 2.

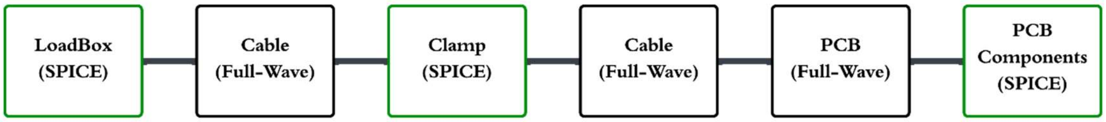
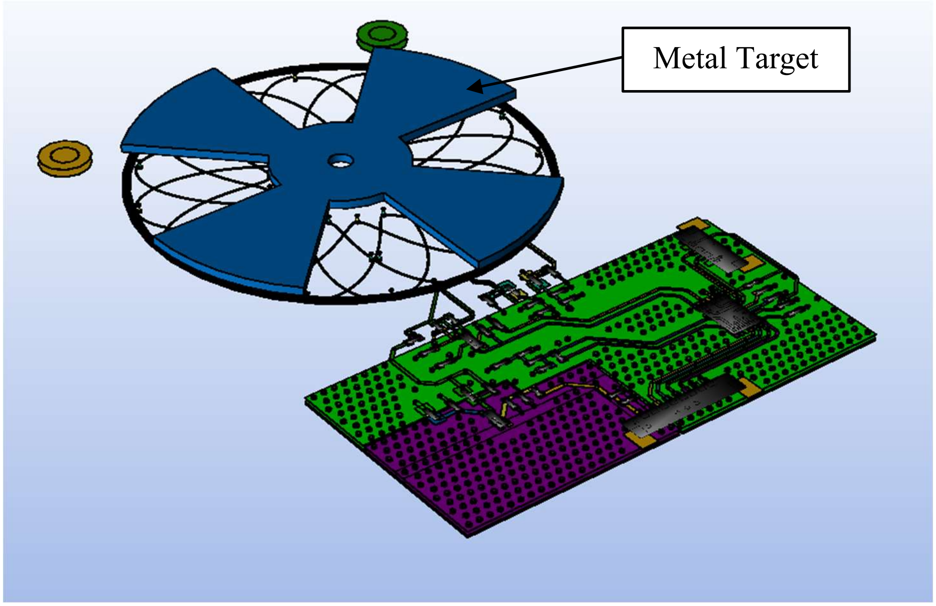
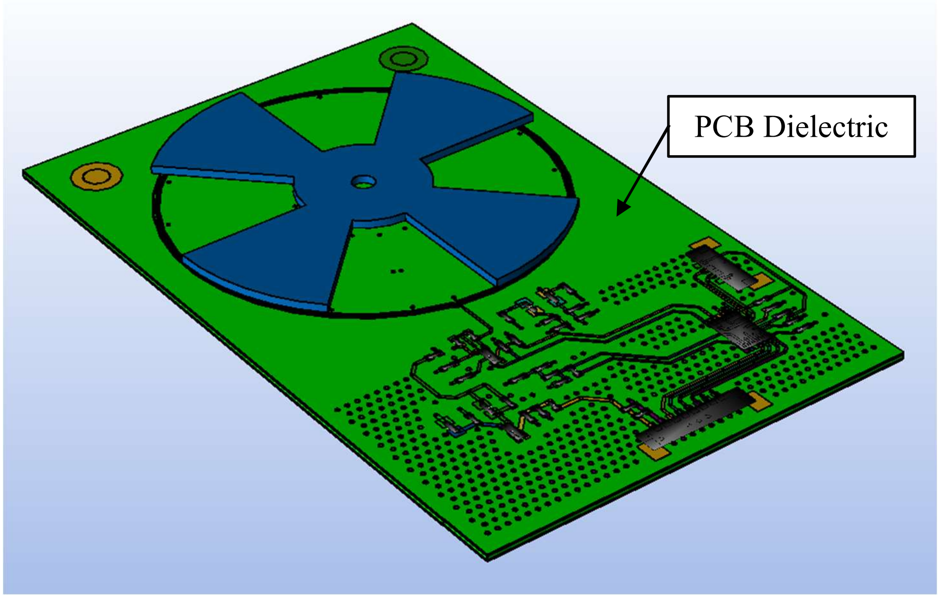


Figure 2. Simulation Models for BCI Setup

The device under test (DUT) for this setup consists of a 90° rotary inductive positioning sensor PCB with a metal target, as shown in Figure 3.



(a)



(b)

Figure 3. 90° Rotary Inductive Positioning Sensor PCB with a Metal Target. (a) Without PCB Dielectric, (b) With PCB Dielectric.

The DUT was evaluated using an open-loop common mode BCI test in accordance with ISO 11452-4, with the current injection clamp positioned 150mm from the DUT. Six cables—comprising four signal cables, one GND cable, and one VIN cable—as shown in Figure 4, were routed through the injection clamp and subjected to Test Severity Level IV, corresponding to an injected clamp current of 200mA.

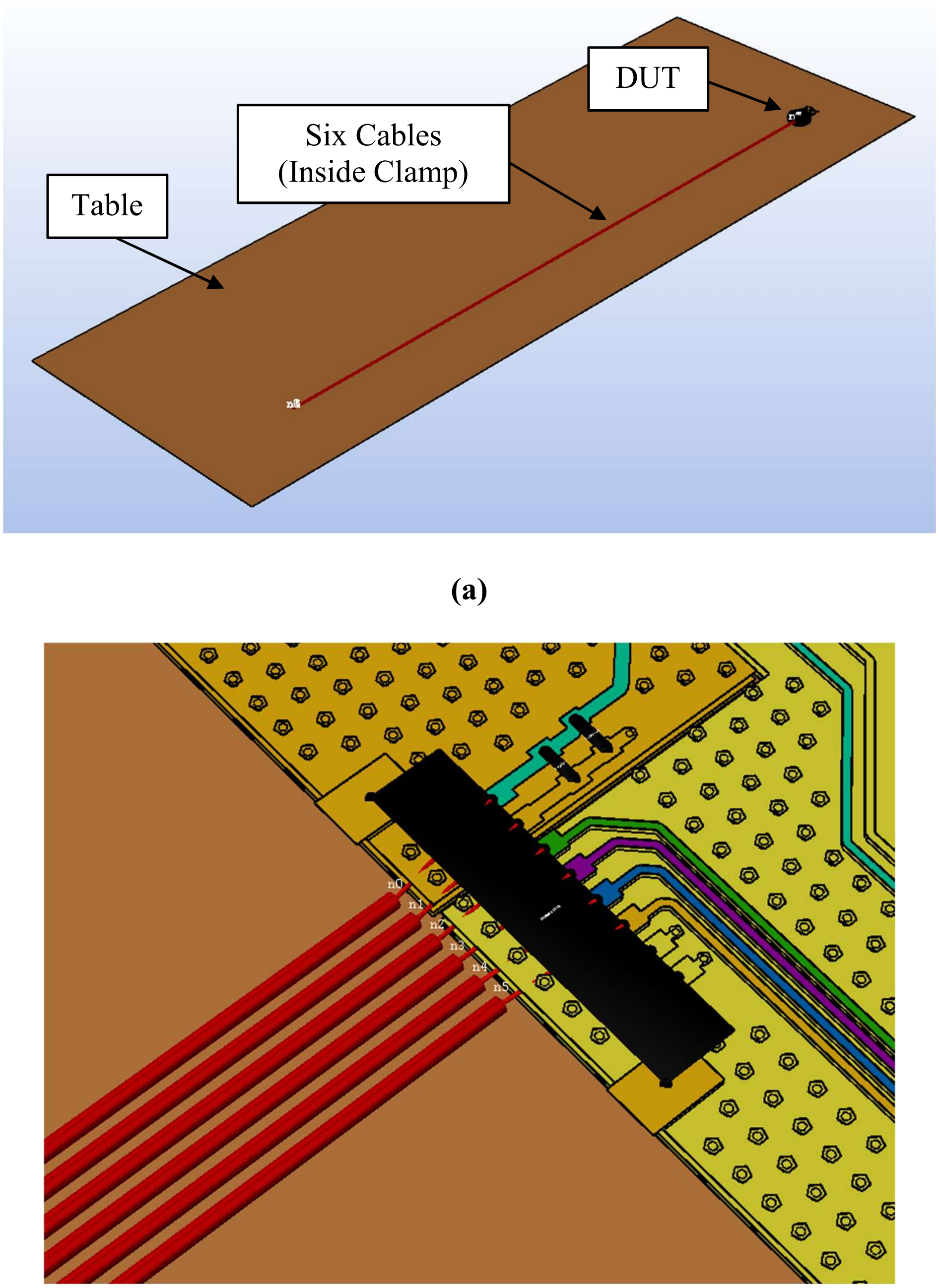


Figure 4. (a). BCI Lab: Cable Setup, **(b).** DUT – Cables Connection (Zoomed In)

The four signal cable terminations were modeled as open circuits to replicate the actual test configuration in which the four cables connect to an oscilloscope through an optical isolator. The GND and VIN cables were connected to two LISNs, which were subsequently connected to a 5V battery, as shown in Figure 5.

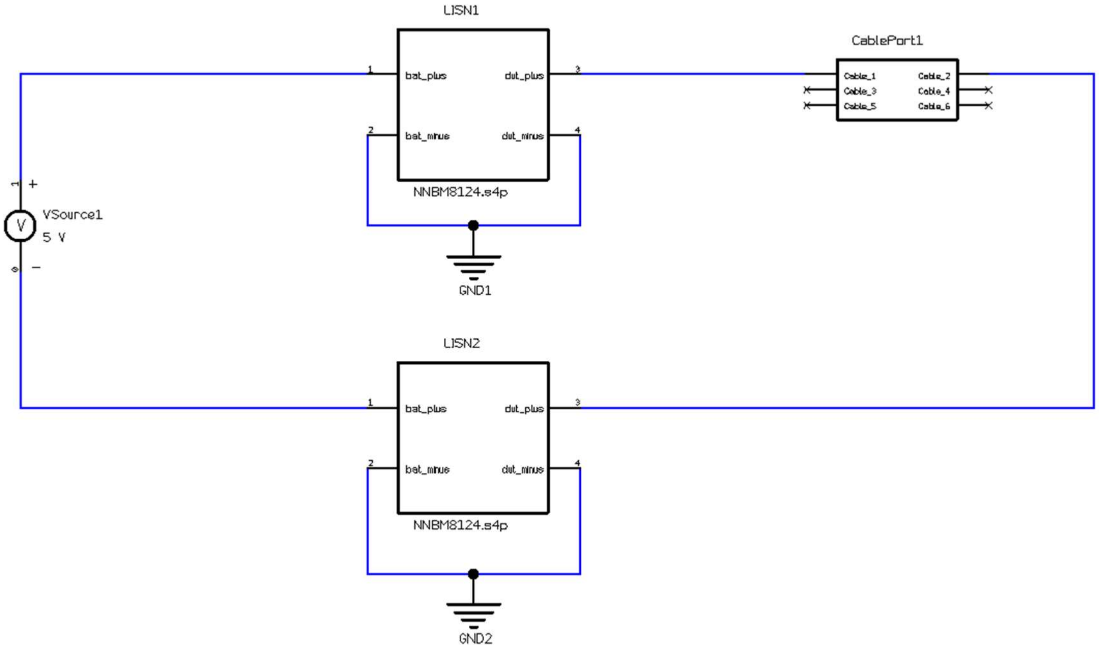


Figure 5. BCI Lab: Load Setup

The cable port shown in Figure 5 depicts the six cables,
Cable 1: VIN cable
Cable 2: GND cable
Cable 3-6: Signal cables (open circuit termination)

IC Pin Voltages

The voltage difference developed at the IC pins is probed during the BCI test. During this test, the differential voltage develops across linear IC impedances (characterized by DPI testing) due to mode conversion. These voltages exhibit resonant voltage peaks across distinct frequency bands, as shown in Figure 6. These bands are of concern for IC pin failures.

An IC pin fails when the induced differential voltage exceeds its immunity threshold at a given frequency (characterized by DPI testing).

From the plot in Figure 6, the IC pin voltage is seen to peak at multiple resonant frequencies. These peaks are distributed across the BCI analysis band, appearing at both low and high frequencies. Depending on the IC pin's voltage immunity at these frequencies, failures may occur.

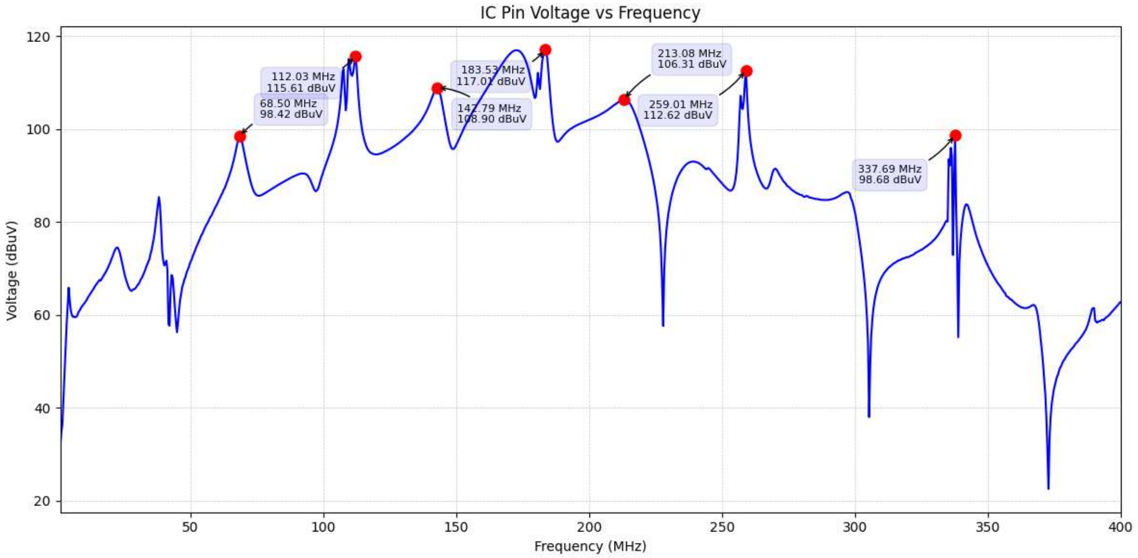


Figure 6. Simulated IC Pin Voltage

Diagnosis

The first step in suppressing the resonant voltage peaks is to identify the discrete PCB components that, along with the board parasitics, contribute to the resonance. This is examined through simulations using two methods: current density analysis and sensitivity analysis.

Current Density Analysis

A current density simulation was performed at the resonant voltage peak frequencies. The resulting current distribution on the PCB is shown in Figure 7.

The figure highlights the high current flow through PCB traces directly connected to the cables. To identify the discrete components contributing to the resonance peaks, primarily within the filtering RC network, the regions of high current density around the filter circuits were examined to determine which components are involved in the resonance. From the current distribution shown in Figure 7, it is observed that the RC filter connected to the secondary coil of the sensor carries a high current at the resonant frequency.

The results from the current density analysis act as a starting point to understand the current flow through the PCB and to identify components that may be resonating and forming dominant current paths.

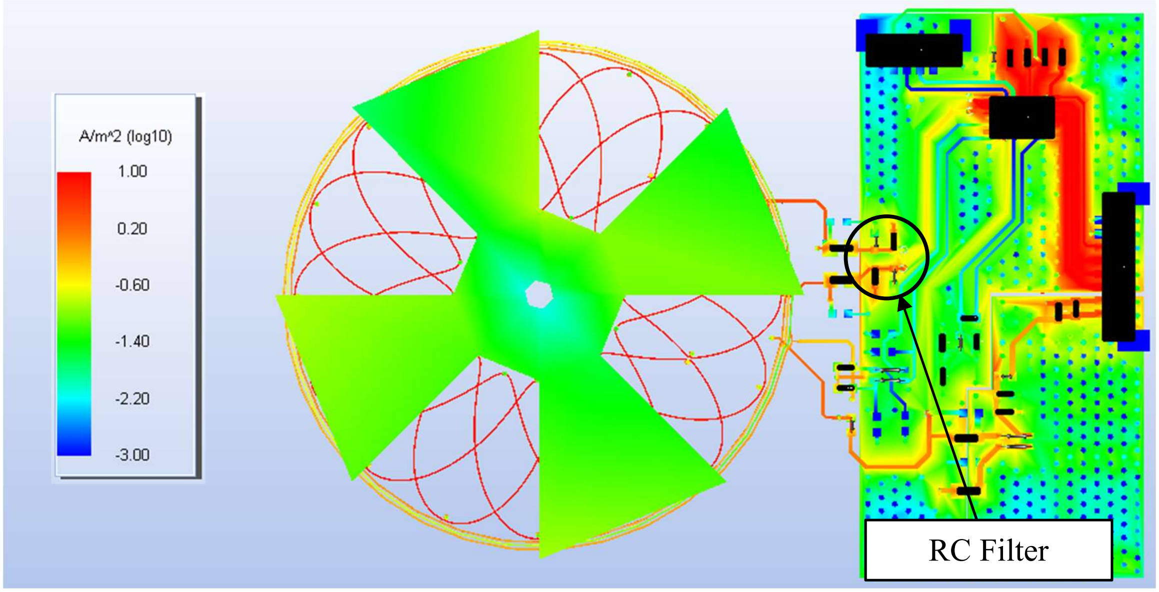


Figure 7. Current Distribution on the PCB

Sensitivity Analysis

In this system, common-mode (CM) noise propagates through the harness to the PCB and then to the primary winding. The noise couples from the primary to the secondary winding and eventually back to the IC pins.

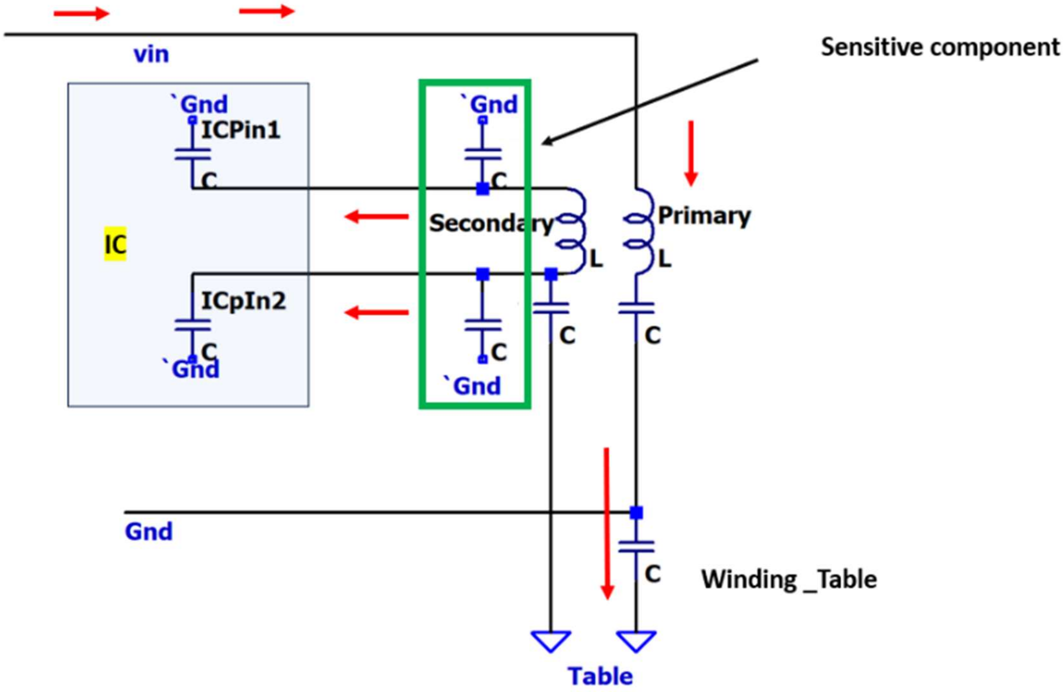


Figure 8. Noise Flow in the System

Because the sensor has large physical dimensions, there is significant capacitance between the sensor and the table, which is critical for CM noise coupling and results in high current on the sensor, as shown in Figure 6. The capacitors connected between the sensor winding and the PCB ground play a crucial role in filtering and mitigating this noise, as shown in Figure 8.

To accurately determine which components influence the IC pin voltage across the BCI analysis band, a sensitivity analysis was performed on the PCB, as described in the ***Sensitivity Analysis for EMI/BCI*** section. The variation in the secondary coil IC pin voltage over frequency was evaluated by applying a ±10% perturbation to the RC filter components (R4 and C19). The voltage variation, indicative of IC pin sensitivity, was then ranked and normalized to provide a comparison of sensitivity across the frequency band.

From the sensitivity analysis shown in Figure 9, the secondary coil IC pin connected to the RC filter exhibits sensitivity to the RC filter across the analysis band. This indicates that adjusting the values of C19 and R4 will have the greatest impact on the IC pin voltage, allowing these components to be tuned to reduce the voltage level.

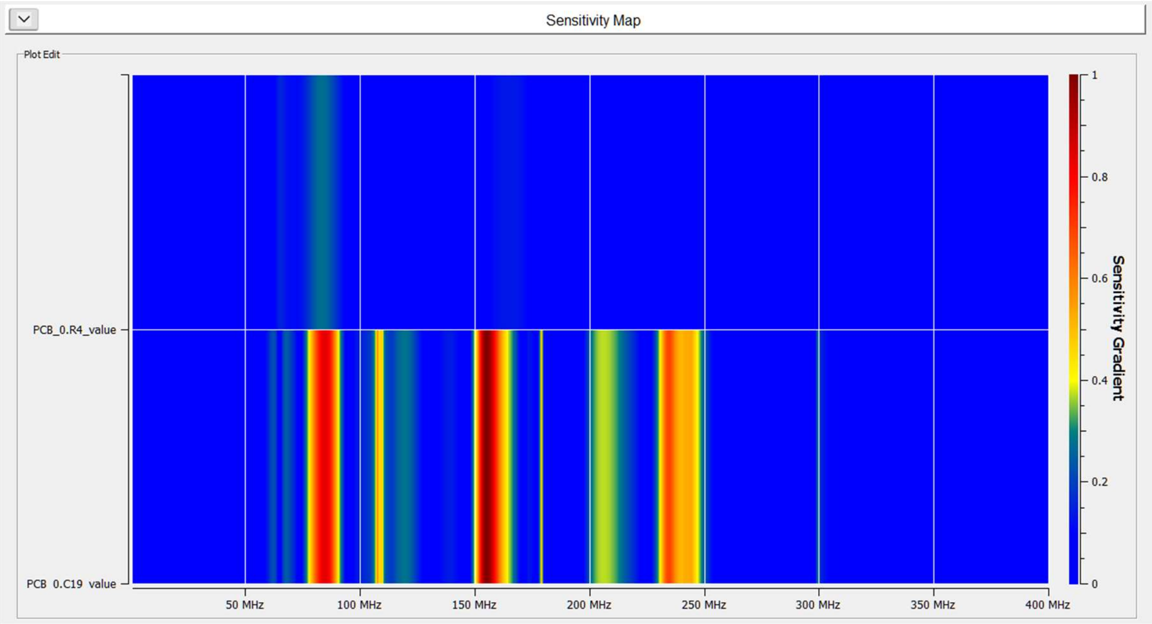


Figure 9. Sensitivity Gradient Plot of IC Pin Voltage

The components influencing the corresponding IC pin voltage have been identified. The next step is to tune their values to reduce the IC pin voltage.

What-If Analysis

Based on the IC pin voltage sensitivity, C19 and R4 define the design space where their values can be tuned to reduce the IC pin voltage. Using the ***What-If*** analysis feature in the simulation tool, the components identified during the sensitivity analysis can be directly replaced with alternative values to observe the resulting voltage behavior without re-simulating the entire setup.

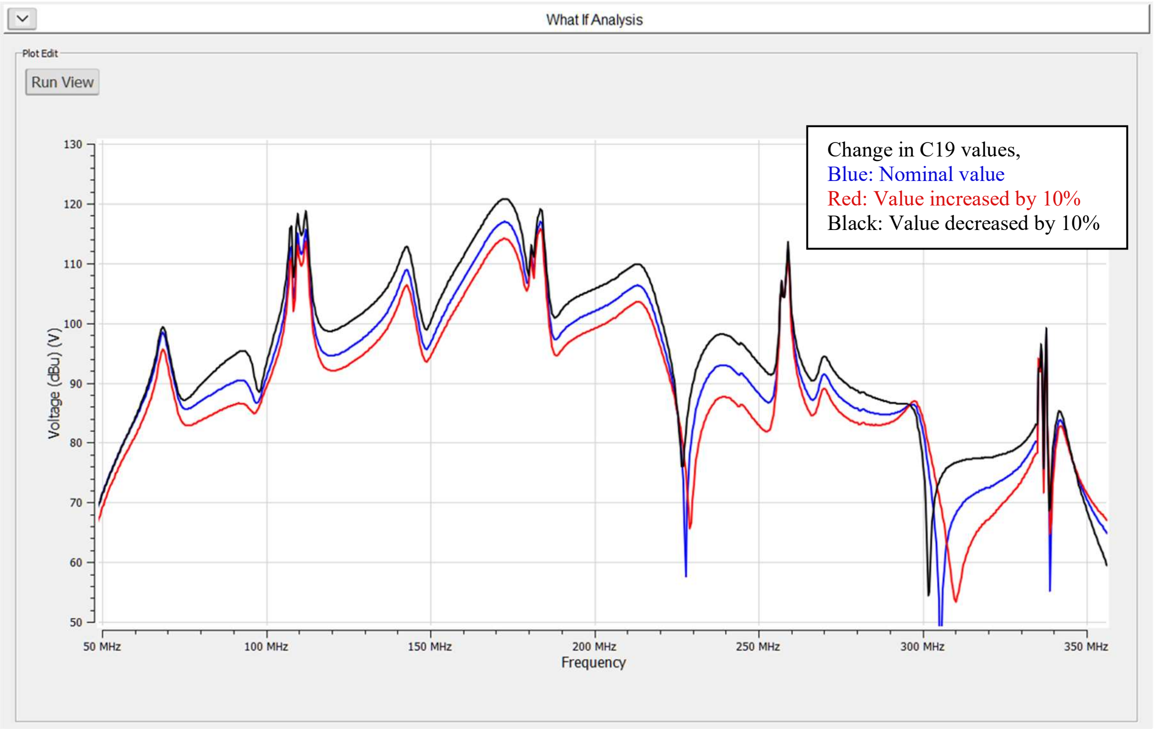


Figure 10. *What-If* Analysis: IC Pin Voltage Change

The *What-If* analysis results for three variations of C19 are shown in Figure 10. It is observed that the secondary coil IC pin voltage decreases with an increase in the filtering capacitor C19 value, while a reduction in C19 results in a higher pin voltage.

This approach can be used to tune the RC filter values to reduce the IC pin voltage and help prevent IC failures.

Conclusion

This paper presented a hybrid modeling approach that combines electromagnetic and circuit-level simulations to evaluate and improve IC immunity in inductive positioning sensor systems. By integrating DPI-based IC immunity models into BCI simulations, the method enables accurate prediction of IC susceptibility to conduct noise at the system level.

Sensitivity and What-If analyses were used to identify and tune key PCB components that influence mode conversion and resonance behavior. The study showed that small adjustments in specific RC filter components can significantly reduce induced IC pin voltages and enhance EMC robustness.

Overall, the proposed methodology provides a practical design tool for early EMC optimization, allowing engineers to predict, diagnose, and mitigate IC-level failures before physical testing.

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